BIO - SKETCH

	Name: Bhaskar Das
	Designation: Assistant Professor
	Total Experience: 10 Years
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Specialization	Deep Learning
Academic Qualification	PhD (Pursuing) in Computer Science & Engineering IIIT, Ranchi
	M. Tech in Information Technology, Assam University (A Central University), Silchar, Result: 8.02 (CGPA), 2013.
	B. Tech in Computer Science & Engineering, West Bengal University of Technology, Result: 7.3 (DGPA), 2009
Total Teaching Experience	10 Years
Publication Details	**International Journals:**
	A. K. Khan, B. Das, H. Sharma, R. K. Pal, T. K. Bayen, "An Algorithm for Floorplanning, Placement and routing in 3D VLSI Through Silicon Vias" in International Journal of Multi-disciplinary Research and Advanced in Engineering, Volume-4, No. IV (October-2012), pp.181-194 (ISSN-0975-7074).
	A. K. Khan, B. Das, T. K. Bayen, "A Review on Channel Routing in VLSI Design" in the IOSR International Journal for computer Engineering, Volumme-5, Issue-I, (ISSN2278-0661(Online), 2278-8727(Print)).
	A. K. Khan, B. Das, T. K. Bayen, "An Efficient Approach for Four-Layer Channel Routing in VLSI Design" in International journal of VLSI Design & Communication System, Volumme-3, No – V (October-2012), pp147-156, (ISSN NO- 0976-1527).
	A. K. Khan, B. Das, S. Roy, "Partitioning in 3D VLSI Physical Design – A Brief Survey" in International Journal of VLSI and Embedded System, (ISSN: 2230-8547; e-ISSN: 2230-8555).

Awards & Honours	
Workshops / Seminars / Conferences / Training Programs Attended	Attended & presented a paper "A Review on Multi- Layer Channel Routing in VLSI Design" at the In 4th International Conference on Information Technology & Business Intelligence (ITBI-12), held at Bhubaneswar, India in 23th -25th , November 2012.
	Attended & presented a paper "A New Algorithm with Minimum Track for Four Layer Channel Routing in VLSI Design" in the IEEE International Conference on Computer Communication and Informatics (ICCCI-2013) at Coimbatore on 4th - 6 th January, 2013.
	Attended & presented a paper "A New Efficient Layer Assignment Algorithm for Partitioning in 3D VLSI Physical Design", in IEEE International Conference in St. Anthony's College, Shilong, on September, 2013.
	Attended & presented a paper "A Technical Survey on Synthesis of Reversible Logic Circuits" in 3rd International conference on Business & Information Management (IEEE) held in NIT, Durgapur on 9th – 11th, January, 2016.
	Attended & presented a paper "Floorplanning in 3-D VLSI Design", in IEEE International Conference on Computing, Cybernetics and Intelligent Information in VIT, Vellore on November, 2013.
Workshops / Seminars / Conferences / Training Programs Conducted	Workshop on "HackIN" (Ethical Hacking and Information Security) held at Department of IT, Assam University, Silchar on 24th – 25th September, 2011.
	1st National Conference on Research & Higher Studies in Information Technology (RHEIT – 2013), Department of IT, Assam University, Silchar on 4 th – 5 th February, 2013.